



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,959	06/27/2003	Gregory N. Henderson	TRQ-12905	3068

22888 7590 11/30/2005

BEVER HOFFMAN & HARMS, LLP  
TRI-VALLEY OFFICE  
1432 CONCANNON BLVD., BLDG. G  
LIVERMORE, CA 94550

EXAMINER

TRAN, PABLO N

ART UNIT	PAPER NUMBER
----------	--------------

2685

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/607,959

Applicant(s)

HENDERSON ET AL.

Examiner

Pablo N. Tran

Art Unit

2685

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 11 August 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☐ Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-35 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 5, 10, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ichihara (6,434,373).

As per claims 1, 5, 10, and 13, Ichihara discloses a circuit having an amplifier comprising a first FET transistor (fig. 5/no. Q11) and a bias circuit having a second FET transistor (fig. 1/no. Q12). Ichihara does not specifically suggest utilized bipolar NPN transistor. However, such is notoriously well known in the art that the examiner takes Official Notice of such. Therefore, it would have been obvious to one of ordinary skill in the art to utilize such bipolar transistors in place of the FET transistors of Ichihara in order to provide a switching circuit that achieves high power conversion efficiency.

The modified circuit of Ichihara further disclose wherein a collector of the first transistor receives a continuously-varying quiescent current from a fixed-level DC voltage source (fig. 5/item Vcc) and a base of the first transistor receives a RF signal to be amplified by the amplifier (fig. 5/no. 15), and wherein the second transistor is in a current mirror with the first transistor (see fig. 5, where it is clear that the base of the

Art Unit: 2685

first coupled to the second transistors, such configuration formed a current mirror transistors, also see specification ([0044-0046]) and biasing the amplifier with a quiescent current that varies proportionally with the voltage signal (abstract, col. 1/n. 48-63, col. 4/n. 44-col. 5/n. 55).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 2-4, 6-9, 11-12, and 14-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ichihara (6,434,373) in view of King (6,137,366).

As per claims 2-3 and 16-18, Ichihara discloses such voltage shifting control circuitry (see Ichihara, fig. 5/no. R1 & C1) but not specifically suggested a voltage shifting resistor T-network. However, such is notoriously well known in the art that the examiner takes Official Notice of such. Therefore, it would have been obvious to one of ordinary skill in the art to utilize such resistor T-network in place of the voltage shifting control circuitry of Ichihara in order to effectively provide proper voltage attenuation to the bias circuit. The modified circuit of Ichihara does not specifically suggest discloses a current mirror. However such is well known in the art, as suggested by King (fig. 5/no. Q5 & Q4). Therefore, it would have been obvious to of ordinary skill in the art to

Art Unit: 2685

provide a current mirror to the bias circuit in order to regulated and provide a stable bias current.

As per claims 4 and 7, the modified apparatus of Ichihara further discloses the claimed limitation as stated above in claim 1.

As per claim 6, 8, and 19-20, the modified apparatus of Ichihara further discloses such voltage shifting control circuitry (see Ichihara, fig. 5/no. R1 & C1, see King, fig. 3/no. R1 & R2) and the amplifier and portion of the bias circuit are together on a single IC [0089] but not explicitly the voltage resistor shifting-network is not on the IC.

However, such circuitry disposition is obvious to one of ordinary skill in the art in order to provide such flexibility to install/replace the appropriated voltage shifting control circuitry depending upon the specific implementation of the bias circuit.

As per claim 9, the modified apparatus of Ichihara further discloses such voltage shifting control circuitry (see Ichihara, fig. 5/no. R1 & C1, see King, fig. 3/no. R1 & R2) but not explicitly a current multiplier. However, such is notoriously well known in the art that the examiner takes Official Notice of such. Therefore, it would have been obvious to one of ordinary skill in the art to utilize such current multiplier to the modified circuitry of Ichihara in order to effectively provide a proper current attenuation to the bias circuit.

As per claims 11 and 15, the modified apparatus of Ichihara further discloses a constant current portion and a continuously varying portion (see King, col. 5/ln. 15-col. 6/ln. 9).

As per claims 12 and 14, the modified apparatus of Ichihara further discloses such current mirror but silent about such non-unity current ratio. However, such is

Art Unit: 2685

notoriously well known in the art that the examiner takes Official Notice of such.

Therefore, it would have been obvious to one of ordinary skill in the art to utilize such current mirror ratio to the modified circuitry of Ichihara in order to effectively provided a proper current attenuation to the bias circuit.

5. Claims 21, 23-25, 27-28, and 30-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Persico et al. (2002/0146993) in view of Ichihara (6,434,373).

As per claims 21, 23, 27-28, and 30-34, Persico et al. disclosed a wireless communication devices having an amplifier (fig. 3/no. 330), a baseband processor (fig. 1/no. 110), and a bias circuit (fig. 3/no. 350). Persico et al. do not specifically suggest such bias circuitry configuration as claimed above in claimed 1. However, such bias circuitry configuration is well known, as suggested by Ichihara (abstract, col. 1/ln. 48-63, col. 4/ln. 44-col. 5/ln. 55). Therefore, it would have been obvious to one of ordinary skill in the art to utilize such bias circuitry configuration of Ichihara in place of the bias circuitry of Persico et al. in order to provide a transmission power control effectively and to lengthen the talk time of the portable telephone.

As per claims 24 and 35, the modified apparatus of Persico et al. further disclose a pre-amplifier (fig. 3/no. 332a).

As per claim 25, the modified apparatus of Persico et al. further disclose a modulator (fig. 1/no. 112).

6. Claims 22, 26, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over the modified circuit of Persico et al. in view of King (6,137,366).

Art Unit: 2685

As per claims 22, the modified apparatus of Persico et al. discloses such voltage shifting control circuitry (see Ichihara, fig. 5/no. R1 & C1) but not specifically suggested a voltage shifting resistor T-network. However, such is notoriously well known in the art that the examiner takes Official Notice of such. Therefore, it would have been obvious to one of ordinary skill in the art to utilize such resistor T-network in place of the voltage shifting control circuitry of the modified circuit of Persico et al. in order to effectively provide proper voltage attenuation to the bias circuit. The modified circuit of Persico et al. does not specifically suggest discloses a current mirror. However such is well known in the art, as suggested by King (fig. 5/no. Q5 & Q4). Therefore, it would have been obvious to of ordinary skill in the art to provide a current mirror to the bias circuit in order to regulated and provide a stable bias current.

As per claim 26, the modified apparatus of Persico et al. further discloses such voltage shifting control circuitry (see Ichihara, fig. 5/no. R1 & C1, see King, fig. 3/no. R1 & R2) and the amplifier and portion of the bias circuit are together on a single IC [0089] but not explicitly the voltage shifting control circuitry is not on the IC. However, such circuitry disposition is obvious to one of ordinary skill in the art in order to provide such flexibility to install/replace the appropriated voltage shifting control circuitry depending upon the specific implementation of the bias circuit.

As per claim 29, the modified apparatus of Persico et al. further discloses a constant current portion and a continuously varying portion (see King, col. 5/ln. 15-col. 6/ln. 9).

***Conclusion***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pablo Tran whose telephone number is (571)272-7898. The examiner normal hours are 9:30 -5:00 (Monday-Friday). If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban, can be reached at (571)272-7899. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-directauspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

November 25, 2005

**PABLO N. TRAN**  
**PRIMARY EXAMINER**

  
AUBOY